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The effect of time-delayed feedback on logical stochastic resonance

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Abstract. We examine the possibility of obtaining logic operation in a quartic-bistable system with linear time-delayed feedback subjected to Gaussian noise. The effect of time-delayed feedback on the effective potential well is investigated, and explicit numerical stimulation is conducted to study the influence of delay time and strength of the time-delayed feedback on the responses of the system. Although the response deteriorates slightly at low values of noise intensity with time-delayed feedback and the peak correct probability decreases from 100% when the delay time is too long, the reliability of obtaining the desired logic output is enhanced in the higher noise boundary with the help of moderate time-delayed feedback. We also found that increasing the linear factor of the system can shift the optimal noise intensity to a higher level.

1 Introduction

Noise exists everywhere, thereby causing difficulty in signal processing. For example, vibration noise hinders fault diagnosis, and underwater noise decreases the accuracy of sonar detection. However, noise is not always detrimental. With careful design, it can be quite useful [1,2]. The interplay of noise and nonlinearity can be quite counterintuitively constructive. One of the most famous examples of the phenomena is stochastic resonance (SR), in which generally feeble input information (such as a weak signal) can be amplified and optimized by the assistance of noise in a nonlinear system [3]. SR has been used in different fields from mechanical systems to neural systems [4,5].

In 2009, Murali et al. applied SR to help designing reconfigurable and reliable logic gates in the presence of noise and introduced the concept of logical stochastic resonance (LSR) [6,7]. As a new idea in nonlinear dynamics, LSR has attracted immense attention from a large number of researchers. The two elements of LSR, namely, nonlinearity and noise, have been widely studied by experts [8–10]. Applications of LSR have been found in tunneling diode [11], rectifier [12], image object detection [13], and synthetic gene networks [14,15], etc.

Time-delayed feedback plays a significant role in many physical systems [16]. Time delay reflects the transmission time related to the transport of matter, energy, and information through the systems [17]. Therefore, time-delayed systems can be regarded as simplified, but very useful, descriptions of systems that involve a reaction chain or a transport process. Thus, a study on the effects of time-delayed feedback has engineering significance. SR with time-delayed feedback in a bistable system has been a subject of several recent papers [18–20]. Specially, delay-aided SR in neural networks has been studied explicitly, such networks include Hodgkin-Huxley neuronal networks [21,22], small-world neuronal networks [23], and FitzHugh-Nagumo neuronal networks [24]. In terms of other implications of delay in noise-driven coupled systems, synchronization [25,26] and signal detection [27] have also been reported. However, how the time-delayed feedback affects LSR phenomenon is still an open question. Moreover, whether new phenomena can be discovered in time-delayed LSR systems is still unclear. We aim to explore this issues in this paper.

In this paper, we demonstrate that OR/AND logic operation can be obtained in a popular quartic-bistable system with time-delayed feedback, analyzing the effect of time-delayed feedback on the responses of the system systematically. The rest of this paper is organized as follows: in Section 2, we describe the model of the bistable system with time-delayed feedback used in this work. In Section 3, the effects of time-delayed feedback on the system are discussed through an explicit numerical stimulation. The paper is discussed and concluded in Section 4.

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2 The bistable system with time-delayed feedback

We consider a system that evolves in double-well potential and is subjected to time-delayed linear feedback loops. The system is described by the following Langevin equation:

$$\dot{x} = -V^{'}(x(t), x(t-\tau)) + r + I(t) + \eta(t) \qquad (1)$$

The bias r has the effect of asymmetrizing the two potential wells. Changing r can morph the logic operation of the system easily. We set $r = 0.3$ to obtain OR/NOR logic and $r = -0.3$ to obtain AND/NAND logic in this paper. However, because the different logic provides the same trend of the effect of time delay, we only choose OR logic to be discussed carefully. $I(t)$ is the low amplitude input signal and consists of two low amplitude input signals $I_1(t)$ and $I_2(t)$, with $I_1(t)$ and $I_2(t)$ encoding two logic inputs (0 or 1) by different values. $I_1(t)$, $I_2(t)$ take the value $-I$ when the logic input is 0 and I when the logic input is 1. I is the amplitude of the low input signal. To facilitate subsequent treatment, I is valued as 0.5. $\eta(t)$ denotes a zero-mean Gaussian white noise with autocorrelation function $\langle\eta(t)\eta(0)\rangle = 2D\delta(t)$, and D is the strength of the noise. $V^{'}(x(t), x(t-\tau))$ is the derivative of the symmetric double-well potential, which is given by

$$V(x(t), x(t-\tau)) = \frac{b}{4}x(t)^4 - \frac{a}{2}x(t)^2 - \frac{c}{x}x(t-\tau)^2 \qquad (2)$$

where a and b are the coefficients of linear and non-linear terms, respectively. c is the linear time-delayed feedback strength. $t(t \leq 0)$ is dropped since it is the same for all variables, and τ is the delay time of the system. The effective potential of equation (2) is given by [28]:

$$V_{eff}(x) = (1 + c\tau)\left(\frac{bx^4}{4} - (a+c)\frac{x^2}{2}\right) \qquad (3)$$

which has three fixed points: an unstable state $x_u = 0$ and two stable states $x_{\pm} = \pm\sqrt{(a+c)/b}$. The effective potential defined by equation (3) is shown in Figure 1. It is shown that the presence of small time-delayed feedback changes the shape of the effective potential. Longer delay time increases the depth of the potential well, while greater time-delayed feedback strength results in a deeper potential well and in a greater distance between the two stable states.

Figure 2 shows the responses of the system to the feeble input, subjected to Gaussian white noise. The uppermost row shows the original signal $I(t)$, which consists of I_1 and I_2. Panel (b) indicates that with high background noise the feeble signal is already overwhelmed. Panels (c−e) show the responses of system without time-delayed and with time-delayed feedback at different delay time, respectively. The output logic is tuned to OR logic. It is clear that the logic output of the system without time-delayed feedback is wrong in the 2nd, 3rd, 7th, and 11th time periods. The outcome is wrong in the 2nd, 5th, 6th, and 11th time periods when the delay time is 80 ms. All the outputs are correct except for only the 2nd time period when the delay time is 10 ms. In this scenario, the presence of moderate time delay enhances the robustness of logic operation. The details of how the time-delayed feedback affects the responses of the system are discussed below.

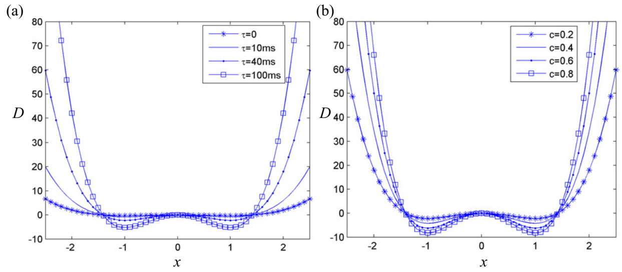

Fig. 1. (a) The effective potential of equation (3) for different time delay τ with $c = 0.2$. (b) The effective potential of equation (3) for different c with $\tau = 40$ ms. Other parameters of the system are set as $a = 0.8$, $b = 1$, $r = 0$, and the density of noise $D = 0$ for both plots.

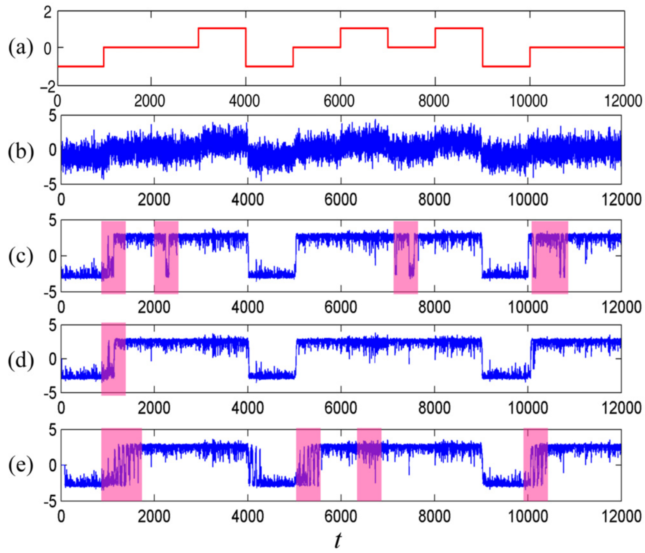

Fig. 2. From top to bottom, (a) shows $I(t)$, (b) shows the input of the system, which is $I(t)$ with noise. The intensity of noise is $D = 1$: (c) shows the response of the nonlinear system without time-delayed feedback to input signal $I(t)$, (d) and (e) show the responses of the system with $\tau = 10$ ms and $\tau = 80$ ms, respectively. Here, other parameters of the system are set as $a = 0.05$, $b = 0.1$, $c = 0.25$, $r = 0.3$, to get OR logic. The wrong result period is also highlighted.

3 Explicit experiment

To show more directly, we calculate the probability of correct logic output P, to evaluate the LSR effect. Modified reference [29] experiment setups, P is obtained as follows: use the random permutated combination of four logical inputs sets $(0, 0)$, $(0, 1)$, $(1, 0)$ and $(1, 1)$ to drive the system for N(in this paper, $N = 200$) runs. In each run, sample $x(t)$ for the four input sets. Calculate the correct probability P_i, the ratio of correct logical output number of sampled $x(t)$ to the total number of sampled $x(t)$, in each run. Specially, in each single input set, the calculation error of $1 \sim 3\%$, which is caused by the relaxation time, is acceptable. In order to reduce the effect of relaxation time, we sample $x(t)$ in different input set with a reasonable time delay. In this strategy, the probability P is given by

$$P = \frac{\sum_{i=1}^{N} P_i}{N}. \quad (4)$$

We first study the interplay of noise intensity D and delay time τ on the effect of obtaining the correct logic gate. The results are displayed in Figure 3. Figure 3a clearly shows that although the peak of correct probability P decreases from 100% for a sufficiently long delay time ($\tau = 100$ ms), the presence of moderate time-delayed feedback ($\tau = 10$ ms and $\tau = 40$ ms) will enlarge the range of the clear logic output to be obtained and is helpful to induce the system to acquire more reliable logic operation under a strong noisy background. Figure 3b evidently shows that when the noise strength is weak ($D < 1$), the nonlinear system with time-delayed feedback yields a clear logic operation for a wide range of delay time and the correct probability decreases from 100% only when the delay time is sufficiently large ($\tau > 50$ ms). The important point here is that, when the background noise is strong ($D = 1$), the correct probability curve (the black line) evolves non-monotonically as the delay time increases. Phenomenon analogous to LSR is obtained.

Furthermore, we study how the system parameters affect the response result [29]. presents an explicit discussion about how the bias coefficient affects system output. In this paper, we mainly focus on discussing about the linear parameters of the system. For fixed delay time $\tau = 10$ ms, we calculate the correct probability of the system with time-delayed feedback at six different linear feedback strengths, while keeping the potential linear parameter $a + c = 0.5$ unchanged. The result is shown in Figure 4a. Figure 4a clearly shows that when we fix the potential linear parameter $a + c$ and modulate only the proportion of these two linear parameters, the shape of the correct probability curve changes little and it shifts in parallel to the right end as the proportion of c increases, which means the system behaves better when the linear time-delayed feedback is the majority linear factor in a strong noisy background, and vice versa. Meanwhile, although the peak probability decreases from 100% when c is sufficiently large ($c = 0.5$), the logic output is still more reliable at a strong noise intensity when the system has a larger linear time-delayed feedback strength. Therefore, we may apply this effect to obtain a more reliable logical output under heavy background noise.

At the same time, Figure 4b shows the correct probability curve when we only change the time-delayed feedback strength c and keep the potential linear variable a fixed. It indicates that the linear factor of the system is very important to get LSR phenomenon. Only when the linear and nonlinear factor are optimally tuned can LSR be obtained.

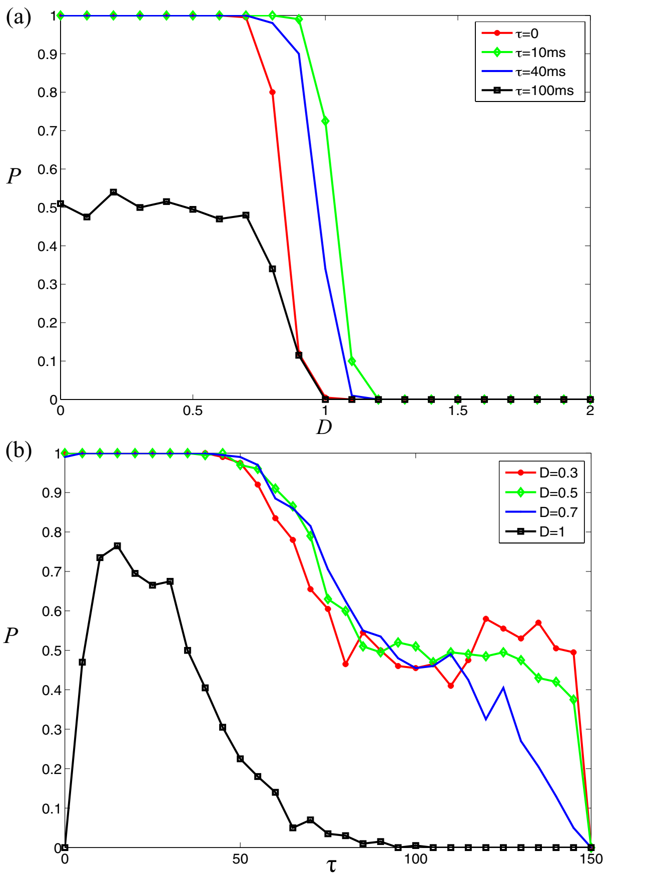

Fig. 3. In OR logic, (a) shows the correct probability P versus noise intensity D at different delay time τ, (b) shows the correct probability P versus delay time τ(ms) at different noise intensity D. The system parameters are set as $a = 0.1$, $b = 0.1$, $r = 0.3$, and the linear strength of feedback is $c = 0.2$.

We stress that the different effects between fixing $a+c$ and fixing a on the response of the system are caused because they have different influences on the effective potential of the nonlinear system. On the one hand, when we keep $a+c$ fixed and only change their proportion, the depth of the barrier is altered, leaving the positions of the two potential wells unchanged. On the other hand, changing c not only alters the depth of the barrier but also changes the distance between the two potential wells.

For the OR logic gate, the success probability P as a function of delay time τ and noise intensity D is plotted in Figure 5, for three different sets of potential parameters. This illustrates thoroughly how the interplay of noise, time delay and system parameters affects the system response. The figure shows that when the linear factor of the potential well is relatively small (Fig. 5a), a wide range of delay time for the system exists, which can obtain clear logic output at weak noisy background ($D < 1$). However, when D is above 1, the system can hardly obtain the correct logic output no matter how the delay time is set. Arising the linear factor of the potential well (Figs. 5b

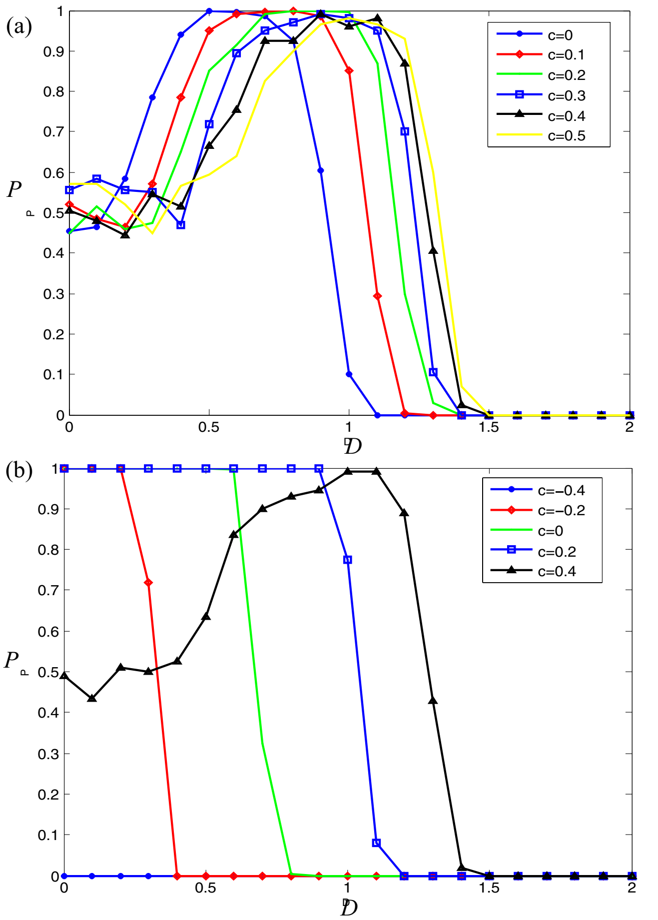

Fig. 4. In OR logic, the correct probability P versus noise intensity D is plotted at different c. Panel (a) shows $a + c$ is fixed as 0.5 and panel (b) shows a fixed as 0.1, respectively. The system parameters are set as $b = 0.1$, $r = 0.3$, and the delay time is 10 ms.

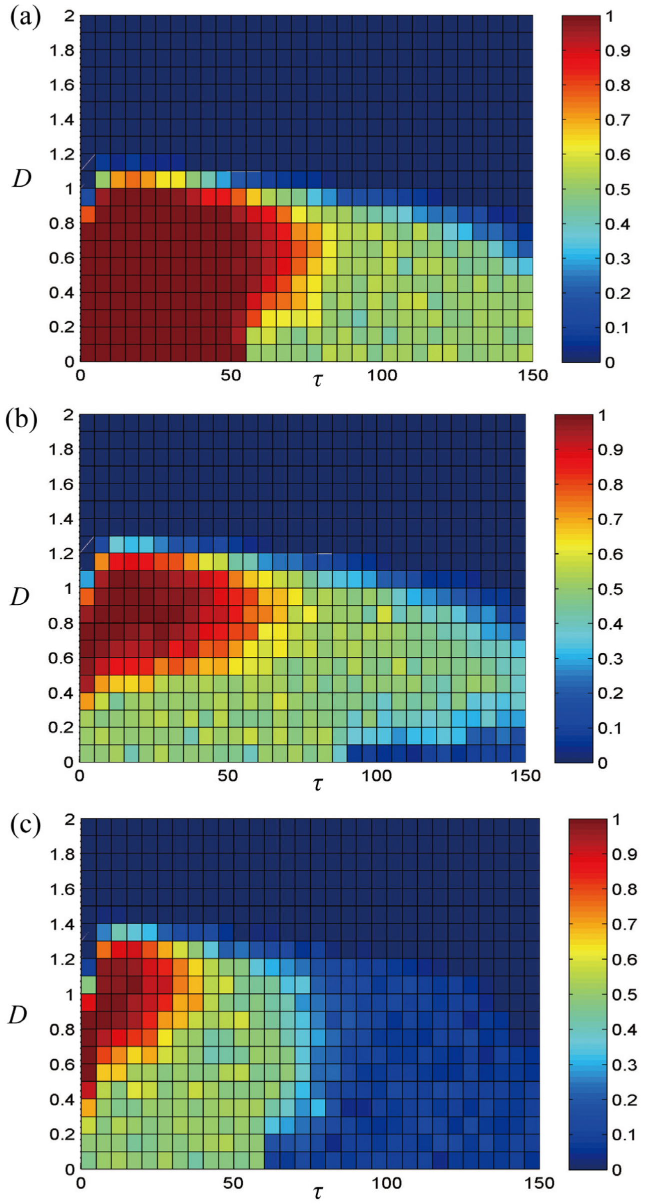

Fig. 5. In a 30×40 lattice, for the OR logic operation, the success probability P versus the delay time τ(x axis) and noise intensity D (y axis) is drawn at three different sets of potential parameters, $a = 0.1$, $c = 0.2$; $a = 0.3$, $c = 0.2$; $a = 0.1$, $c = 0.4$, respectively, from top to bottom. Other parameters are set as $b = 0.1$ and $r = 0.3$.

and 5c), no matter we increase c or increase a, the system behaves better at strong noisy background, but the area where the correct probability is 100% in the plate becomes narrower. On the one hand, when $a > c$, the optimal window of the delay time is wider than it is when $a < c$. On the other hand, the peak correct probability of getting the desired logic output is higher when c is the major factor at strong noise intensity.

4 Conclusion

In this paper, we have demonstrated that a quartic-bistable system which has time-delayed feedback can perform as logic gate, especially OR logic operation. The presence of time-delayed feedback raise the barrier of the effective potential and change the nonlinearity of the system consequentially. Explicit numerical stimulation is carried out to analyze the effect of delay time and linear strength of the time-delayed feedback on the responses of the system to feeble input in the presence of Gaussian noise. The correct probability P of obtaining the desired logic output is calculated to quantify the consistency.

The existence of moderate delay time feedback may serve as a constructive role to yield a more robust logic operation in a strong noisy background. In this scenario, the reliability of the logic system can evolve non-monotonically as a function of delay time. When the delay time is too long, the reliability of obtaining right logic output is broken. In [30], an adaptive LSR obtained by tuning periodic forcing is proposed. In this paper, we propose another method to obtain adaptive LSR. In the time-delayed feedback nonlinear system, we can first examine the noise intensity, and then adjust the delay time or the linear factor of the potential well and modulate the nonlinear dynamics to the best state to obtain robust logic operation. The results presented here are quite general and can be used to design adaptive logic gates.

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Author contribution statement

All the authors were involved in the preparation of the manuscript. All the authors have read and approved the final manuscript.

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